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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PENDLETON, BRIAN T	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 11/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/788,282	BORGATTI ET AL.	
	Examiner	Art Unit	
	Brian T. Pendleton	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 9/5/06 have been fully considered but they are not persuasive. Applicant asserts that claims 23-25 are enabled by the specification and therefore the 112, 1st paragraph rejection should be withdrawn. Examiner disagrees. The argument by the Applicant is that page 4 states that the non-volatile memory 5 adapts the format of blocks or packets of data. That lone passage does not enable the invention. There is no language that describes what formatting is being accomplished. The rejection is maintained. Furthermore, Applicant alleges that Naim does not discloses a single chip of semiconductor material comprising the transmission line, non-volatile memory, signal-conversion unit, and control unit with regard to claim 1. Specifically, it is alleged that Naim only discloses a single substrate, which is a printed circuit board. Examiner disagrees with that characterization of the reference. A printed circuit board contains one piece of semiconductor material. The circuit board of Naim contains all the claimed limitations, such as the memory, controller, transmission line, and signal-conversion unit. The rejection is maintained. With regard to the dependent claims, the respective rejections are maintained as Applicant has only argued that the secondary references do not cure the deficiencies of Naim, nevertheless it is the Examiner's contention that Naim does not contain any deficiencies.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 23-25 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant recites an "format adapter" which is not described in the specification as a separate discrete element involved in the storage of compressed audio signals. Examiner is determining the merits of the claims with the interpretation that a "format adapter" stores the compressed audio signals in memory locations.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3 and 23-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Naim. Naim discloses a portable audio recording device and player comprising control unit (DSP 4), signal conversion unit having D/A converter 20, A/D converter 21, and non-volatile memory 8 in figure 1B. As taught in column 4 lines 56-67, the portable device has a single substrate for supporting the player and hard disk 3 (see also figure 3a). The single substrate reads on a chip of semiconductor material in which an inherent main transmission line resides. Column 2 lines 40-52 and column 3 lines 42-48 disclose that the player can record audio through converting the

analog signal to a digital signal and reproducing the audio signal through converting the digital signal to an analog signal. Column 5 lines 1-20 teach that the digitalized signal is compressed, indicating that the conversion from digital to analog involves decompression. Claims 1-3 are rejected. Per claims 23-25, inherently there is a format adapter for storing the compressed audio signals in memory 8, as the digital signals could not be stored without adapting them to the memory's internal structure.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 4, 5, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naim in view of Unno et al. Naim does not disclose that the signal-conversion unit has temporary storage means coupled to a converter circuit. Naim et al has a converter circuit for compressing the audio signals. The use of a temporary storage means was well known in the art, as evidenced by Unno et al. Unno et al taught an audio player and recorder having a buffer memory 6 which temporarily stores data received from the compressor 4 (first stream) and data read from the flash memory 8 (second stream). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the teachings of Unno et al in the Naim and include a buffer memory after the compressor. Claim 4 is rejected. Regarding method claim 12, the combination reads on the claim limitations. Specifically, Naim has a microphone for receiving an input analog signal correlated to a voice signal, compression means for compressing the input analog signal resulting in a stream of compressed digital signals. Naim also teaches a single integrated circuit chip. Unno et al is relied upon for sending the compressed digital

signals to a temporary storage means (buffer memory 6). The compressed digital signals are then sent from buffer memory to the non-volatile memory 8 of Naim. During playback, a second stream of compressed digital signals are sent from non-volatile memory 8 to the converter circuit and subsequently to decompression means for decompressing the second stream and generating an output analog signal. As to claims 5 and 13, Unno et al taught that the compression means generates blocks of digital samples having a fixed dimension in column 7.

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naim in view of Unno as applied to claim 5 above, and further in view of Daberko. The combination of Naim and Unno et al teach an apparatus comprising a semiconductor chip, bus, control unit, signal-conversion unit having a microphone, compression means, fetching means, decompression means, a non-volatile memory unit wherein the signal-conversion unit has temporary storage means coupled to a converter circuit. The combination does not teach that the temporary storage means has first and second memory buffers whereby the signal conversion unit controls transfer of digital signals alternately to the first and second memory buffers. Daberko teaches a non-volatile memory (flash) having first and second memory buffers in figure 3C. As suggested in column 9 lines 44-55, it was advantageous to allow the buffers to switch tasks. One memory buffer can be disseminated or unloaded while the other memory buffer is written to primary memory. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate first and second memory buffers in the combination of Naim and Unno et al. Regarding claim 7, it was well known to use RAM as memory buffers.

Claims 8 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naim in view of Unno et al as applied to claims 5 and 12 above, and further in view of Rossum. The

combination does not teach that the temporary storage means has first and second memory buffers whereby the signal conversion unit controls transfer of digital signals alternately to the first and second memory buffers and that the control means of the signal conversion unit transfers first blocks of digital signals to the first memory buffer, detects filling of the first memory buffer, transfers second blocks of digital signals to the second memory buffer and sends the first blocks to the non-volatile memory unit, detects filling of the second memory buffer and transfers third blocks of digital signals to the first memory buffer and sends the second blocks to the non-volatile memory unit. To an ordinarily skilled artisan, this feature is known as "ping-pong" buffering. The combination of Naim and Unno et al while supplying a buffer, does not explicitly teach "ping-pong" buffering. However, this feature was well known in the art, as evidenced by Rossum. Column 1 lines 12-26 taught the art of ping-pong buffering noting that when a first buffer is full then a second buffer is filled and the data from the first buffer is processed. This process is repeated when the second buffer is full and control is passed back to the first buffer. Thus, there was taught alternating between two buffers and detecting filling of each of the buffers. The buffers were examined to see if they were full since control is passed to the other buffer when one is full. It would have been obvious to one of ordinary skill in the art at the time of invention to use the feature of "ping-pong" buffering in the combination of Naim and Unno et al.

Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naim in view of Ogawa. Naim does not explicitly teach that the memory device has a first memory area storing digital signals and a second memory area containing information regarding occupation of memory locations of the first memory area. Ogawa discloses a flash EEPROM management

system. The system has a flash ROM 15 having a management area and data area for storing digital signals. See figures 4 and 5a-c. As discussed in the "Summary of the Invention" section, column 2, the management area stores state information indicating whether a corresponding data area is used, unused or busy. Thus, it was well known to have a memory containing data signals and information regarding occupation (used/unused flags) of the memory locations containing data signals. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Ogawa in the invention of Naim and have a first memory area for data and a second memory area for data management of the data in the first memory area. Claim 9 is rejected. As to claim 10, the first sub-area is the used state flag 156 and it is inherent that another sub-area contains read-sequence pointers. Regarding claim 11, Official Notice is taken that the use and advantages of multi-level flash EEPROMS were notoriously well known in the art of digital signal storage and one of ordinary skill in the art would have been motivated to use them.

Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naim in view of Unno et al. Naim teaches an apparatus comprising an inherent bus (main transmission line), control unit (DSP), converter circuit having compression means for generating a first stream of compressed digital signals and decompression means for decompressing a second stream of compressed digital signals and generating an output analog signal, non-volatile memory unit 8 coupled to the bus for storing compressed digital signals and for generating a second stream of compressed digital signals according to control signals from control unit. Naim also discloses that the control unit, memory unit, signal conversion unit and transmission line are integrated in a single chip of semiconductor material. As discussed above, it would have been

obvious to include temporary storage means in the Naim per the teachings of Unno et al. Unno et al teach temporary storage means having first and second memory buffers for sequentially receiving first and second streams of compressed data for input into flash memory. As to claim 16, inherently the converter circuit generates blocks of digital data for storage in the memory.

Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naim in view of Unno et al as applied to claim 16 above, and further in view of Rossum. The combination of Naim and Unno et al does not teach that the signal conversion unit controls transfer of digital signals alternately to the first and second memory buffers and that the control means of the signal conversion unit transfers first blocks of digital signals to the first memory buffer, detects filling of the first memory buffer, transfers second blocks of digital signals to the second memory buffer and sends the first blocks to the non-volatile memory unit, detects filling of the second memory buffer and transfers third blocks of digital signals to the first memory buffer and sends the second blocks to the non-volatile memory unit. To an ordinarily skilled artisan, this feature is known as "ping-pong" buffering. The combination of Walters et al and Unno et al while supplying a buffer, does not explicitly teach "ping-pong" buffering. However, this feature was well known in the art, as evidenced by Rossum. Column 1 lines 12-26 taught the art of ping-pong buffering noting that when a first buffer is full then a second buffer is filled and the data from the first buffer is processed. This process is repeated when the second buffer is full and control is passed back to the first buffer. Thus, there was taught alternating between two buffers and detecting filling of each of the buffers. The buffers were examined to see if they were full since control is passed to the other buffer when one is full. It would have been obvious to one of ordinary skill in the art at the time of invention to use the feature of "ping-pong"

buffering in the combination of Walters, Norris and Unno et al. Claim 17 is met since the teaching of alternating between two buffers was suggested by Rossum. Regarding claim 18, it was well known to use RAM as memory buffers. Claim 19 is met since Rossum taught detecting filling of the memory buffers.

Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naim in view of Unno et al, as applied to claim 15 above, and further in view of Ogawa. The combination does not teach that the memory device has a first memory area storing digital signals and a second memory area containing information regarding occupation of memory locations of the first memory area. Ogawa discloses a flash EEPROM management system. The system has a flash ROM 15 having a management area and data area for storing digital signals. See figures 4 and 5a-c. As discussed in the "Summary of the Invention" section, column 2, the management area stores state information indicating whether a corresponding data area is used, unused or busy. Thus, it was well known to have a memory containing data signals and information regarding occupation (used/unused flags) of the memory locations containing data signals. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Ogawa in the invention described by Naim and Unno et al and have a first memory area for data and a second memory area for data management of the data in the first memory area. Claim 20 is met. As to claim 21, the first sub-area is the used state flag 156 and it is inherent that another sub-area contains read-sequence pointers. Regarding claim 22, Examiner takes Official Notice that it was obvious to use multi-level flash EEPROMS as they were well known in the art of digital signal storage.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian T. Pendleton whose telephone number is (571) 272-7527. The examiner can normally be reached on M-F 7-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian Chin can be reached on (571) 272-7848. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Brian T. Pendleton
Primary Examiner
Art Unit 2615

btp